ABSTRACT

Disclosed is a synchronous information storage device that uses a synchronizing clock signal to exercise operation timing control and processes operations with high efficiency to improve performance and provide low power consumption, which is characteristic of DRAMs. The information storage device includes a plurality of memory cells for storing data by accumulating an electrical charge and an amplifier for amplifying the electrical charge of the memory cells, and uses a synchronizing clock signal for input/output timing of the data. An electrical charge removal operation for moving an electrical charge from the memory cells to the amplifier or an electrical charge accumulation operation for acquiring an electrical charge from the amplifier and accumulating the electrical charge in the memory cells and an input/output operation for the amplifier in relation to the outside of the information storage device are processed while using a single clock of the synchronizing clock signal for synchronization timing.